COURSE DESCRIPTION CARD - SYLLABUS

Course name
Nanometer CMOS technologies

Course

Field of study
Computing

Year/Semester
2/4

Area of study (specialization)
-

Profile of study
general academic

Level of study
First-cycle studies

Course offered in
polish

Form of study
part-time

Requirements
elective

Number of hours

Lecture
12

Laboratory classes
12

Other (e.g. online)
0

Tutorials
0

Projects/seminars
0

Number of credit points

3

Lecturers

Responsible for the course/lecturer:
dr hab. inż. Szymon Szczęsny

Responsible for the course/lecturer:
mgr inż. Damian Huderek

Prerequisites

The student starting this course should have knowledge of discrete mathematics, logic and digital electronics. He should have the ability to solve basic problems of algorithmics, obtain information from indicated sources and build simple electronic systems. They should understand the need to expand their competences in the field of modeling real decision problems and using IT tools to solve them. In addition, in terms of social competences, the student must present attitudes such as honesty, responsibility, perseverance, cognitive curiosity, creativity, personal culture, respect for other people.

Course objective

The overall goal is to present the entire process of designing integrated circuits using modern nanometer technology. In particular, the following issues will be discussed:

1. Discussion of the current trends in the microelectronics market, especially in the area of nanometer semiconductor technologies and alternative technologies, eg carbon ones.

2. Acquainting with professional commercial tools for designing the hardware layer of an information system, integrated with exemplary commercial nanometer technologies.

3. Overview of the path "from transistor to processor", ie showing the full process of designing a digital CMOS circuit with a simulation of its operation at each stage of the process.

4. Presentation of methods of realization of discrete and logic functions using integrated circuits.

5. Realization of ASIC topography with scatter analysis in fabrication processes.

Course-related learning outcomes

Knowledge

1. Student has ordered and theoretically founded general knowledge in the field of key issues of computer science, and detailed knowledge in the field of selected issues in this discipline of science

2. Student has knowledge about important directions of development and the most important achievements of computer science and other related scientific disciplines, in particular electronics, telecommunications as well as automation and robotics

3. Student knows the basic techniques, methods and tools used in the process of solving IT tasks, mainly of an engineering nature, in the field of key IT issues

Skills

1. Studentcan obtain information from various sources, including literature and databases, both in Polish and in English, integrate them properly, interpret and critically evaluate them, draw conclusions, and comprehensively justify their opinions

2. Student can properly use information and communication techniques, applicable at various stages of the implementation of IT projects

3. Student is able to formulate and solve IT tasks, apply appropriately selected methods, including analytical, simulation or experimental methods

4. Student can - in accordance with the given specification - design and implement a device or a broadly understood IT system, selecting a programming language appropriate for a given programming task and using appropriate methods, techniques and tools

5. Student is able to plan and implement the process of own permanent learning and knows the possibilities of further education (second and third degree studies, postgraduate studies, courses and exams conducted by universities, companies and professional organizations)

Social competences

1. Student understands that in computer science knowledge and skills very quickly become obsolete

2. Student is aware of the importance of knowledge in solving engineering problems and knows examples and understands the causes of malfunctioning information systems that have led to serious financial and social losses or to serious loss of health and even life

Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:

The learning outcomes presented above are verified as follows:

Formative assessment:

a) in the field of lectures:

- on the basis of answers to questions about the material discussed in the lectures.

b) in the field of laboratories / exercises:

- based on the assessment of the current progress in the implementation of tasks.

Summative assessment:

a) in the field of lectures, verification of the assumed learning outcomes is carried out by:

- assessment of the knowledge and skills demonstrated on the written test with different characteristics of problems to be solved: multiple-choice test questions, content to be completed, simple computational or algorithmic tasks and problem tasks of greater complexity; pass on condition of obtaining more than half of points.

- discussion of the credit results,

b) in the field of laboratories / exercises, verification of the assumed learning outcomes is carried out by:

- assessment of knowledge and skills related to the implementation of laboratory tasks through a colloquium,

- evaluation of reports prepared partly during the classes and partly after their completion; this assessment also includes the ability to work in a team,

- assessment of skills related to the implementation of laboratory exercises

Obtaining additional points for activity during classes, especially for:

- discussion of additional aspects of the issue,

- the effectiveness of applying the acquired knowledge while solving a given problem,

- the ability to cooperate as part of a team practically carrying out a detailed task in the laboratory

Programme content

The lecture covers the following issues:

1. Trends, directions of development and limitations of the microelectronics industry.

2. Characteristics of modern semiconductor technologies, integrated circuits market, review of alternative technologies (carbon, magnetic, etc.).

3. Parameters of the hardware layer of IoT systems, challenges faced by VLSI designers.

4. Review of ASIC design tools, functionality of Mentor Graphics tools. Functionality of SPICE languages.

5. Models of MOS transistors and their use in designing digital circuits.

6. Digital techniques and implementation of basic digital computing modules.

7. Complex MOS structures? finger transistors, waffle transistors, interdigitated and common centroid transistors. Designing memory.

8. Static and dynamic parameters of digital circuits, optimization of computing power and calibration of power consumption.

9. How to prepare the system for fabrication? Overview of DRC, ERC, LVS, PEX verification methods; problem of parameter dispersion in fabrication, methods of prediction of dispersion and evaluation of the sensitivity of semiconductor structures, DFT (Design For Testing) strategy.

10. Design of integrated circuit topography, row strategies. Management of metallic layers. AMPLE language for topography design automation.

11. Hardware acceleration, implementation of preprocessors on the example of commercial solutions, problems of parallelization of calculations. Hardware implementations of compression, sharpening and classification algorithms.

12. Semiconductor structures of neural networks, neuroprocessors, problems of parallelization and pipelines in neural networks, neuroprocessor-brain interface on the example of artificial hippocampus and artificial perikaryons.

13. 0.5 V, 0.3 V, 0.2 V techniques - integrated circuits operating at reduced supply voltage. Voltage mode vs. current mode? computing systems in 40 nm and smaller technologies.

14. Routing of power signals and digital signals. Time parameters of paths, parasitic elements. CMOS vs. PCB? comparison of scale, problems, tools.

15. Oscillators, pad time parameters, oscilloscope probes capacity compensation. System testing.

16. Discussion of the latest achievements and current problems in the field of microelectronics on the basis of the current scientific literature. Presentation of research work carried out at the university.

The laboratory covers the following issues:

1. Acquainting with Mentor Graphics' Design Architect / Pyxis Schematic tools used to design integrated circuits, mainly digital circuits at the schematic stage.

2. Acquainting with the specification of the selected semiconductor technology used during laboratory classes.

3. Simulation of operation of single MOS transistors implemented in selected nanometer technologies.

4. Building and analysis of a simple logic gate implemented with the use of MOS transistors.

5. Acquaintance with the selected language of hardware layer architecture description.

6. Examination of a complex ASIC, evaluation of its computing power and analysis of time parameters.

7. Acquainting with ICStation / Pyxis Layout and CALIBRE tools by Mentor Graphics for designing and verifying the layout of the integrated circuit.

8. Layout design of the selected digital layout along with DRC, LVS, PEX verification and post-layout simulation of its operation

Teaching methods

1. Lecture: multimedia presentation supplemented with examples given on the blackboard

2. Laboratory exercises: problem solving, practical exercises, data analysis, simulation, discussion, team work, case studies, multimedia show.

Bibliography

Basic

1. "Podstawy elektroniki cyfrowej", Józef Kalisz, WKŁ, Warszawa, 2007

2. "Mixed-Signal Systems A Guide to CMOS Circuit Design", A. Handkiewicz, A Wiley-Interscience Publication John Wiley & Sons, INC., 2002

3. "CMOS, Circuit Design, Layout, and Simulation", R. Jacob Baker, A John Wiley & Sons, Inc., Publication, 2010

Additional

1. "CMOS IC LAYOUT Concepts, Methodologies, and Tools", Dan Clein, Library of Congress Cataloging-in-Publication Data, ISBN 0-7506-7194-7

2. "Projektowanie układów scalonych CMOS", A. Gołda, A. Kos, WKŁ, Warszawa, 2011

3. A. Handkiewicz, S. Szczęsny, M. Naumowicz, P. Katarzyński, M. Melosik, P. Śniatała, M. Kropidłowski, "SI-Studio, a layout generator of current mode circuits", Expert Systems with Applications, vol. 42, Issue 6, pp. 3205-3218, 2015

4. S. Szczęsny, "0.3 V 2.5 nW per Channel Current-Mode CMOS Perceptron for Biomedical Signal Processing in Amperometry", IEEE Sensors Journal, vol. 17, Issue 17, pp. 5399-5409, 2017

Breakdown of average student's workload

	Hours	ECTS
Total workload	40	3,0
Classes requiring direct contact with the teacher	24	2,0
Student's own work (literature studies, preparation for laboratory classes, preparation for tests) [1]	16	1,0

[1] delete or add other activities as appropriate